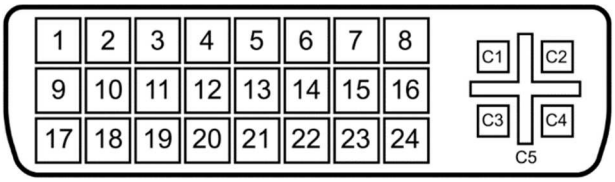
Rev. 1.2 10.2020

SOPHIA 2

Improved Graphics Television Interface Adapter

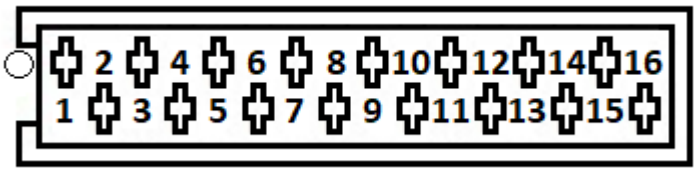
1. DVI-I Output Connector



1 – TMDS Data 2 -
2 – TMDS Data 2 +
3 – TMDS Data 2 Shield
4 – NC
5 – NC
6 – NC
7 – NC
8 – VSYNC/ RGB Blanking
9 – TMDS Data 1 -
10 – TMDS Data 1 +
11 – TMDS Data 1 Shield
12 – NC
13 – NC
14 - +5V 150mA max.
15 – GND
16 – Hot Plug Detect
17 – TMDS Data 0 -
18 – TMDS Data 0 +
19 – TMDS Data 0 Shield
20 – NC
21 – NC
22 – TMDS Clock Shield
23 – TMDS Clock +
24 – TMDS Clock -

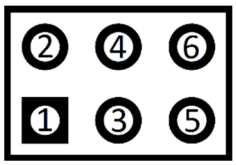
C1 – Analog Red
C2 – Analog Green
C3 – Analog Blue
C4 – HSYNC/CSYNC
C5 – Analog GND

2. Board-To-Board Connector



1 – Analog Blue
2 – Analog VSYNC
3 – Analog Green
4 – Analog HSYNC/CSYNC
5 – Analog Red
6 – GND
7 – GND
8 – +5V Out
9 – TMDS Data 2 +
10 – TMDS Data 2 -
11 – TMDS Data 1 +
12 – TMDS Data 1 -
13 – TMDS Data 0 +
14 – TMDS Data 0 -
15 – TMDS Clock +
16 – TMDS Clock -

3. JTAG Connector



1 – TDI
2 – TMS
3 – TDO
4 – TCK
5 – +3.3V
6 – GND

4. REGISTERS

DISM0PF $D000 (R/W)
DISM1PF $D001 (R/W)
DISM2PF $D002 (R/W)
DISM3PF $D003 (R/W)
DISP0PF $D004 (R/W)
DISP1PF $D005 (R/W)
DISP2PF $D006 (R/W)
DISP3PF $D007 (R/W)
DISM0P $D008 (R/W)
DISM1P $D009 (R/W)
DISM2P $D00A (R/W)
DISM3P $D00B (R/W)
DISP0P $D00C (R/W)
DISP1P $D00D (R/W)
DISP2P $D00E (R/W)
DISP3P $D00F (R/W)

These registers disable (when the corresponding bit is set) independently each collision, respectively to the collision registers. Only 4 lower bits of each register are used. Default value of each register is 00h. These flags can only be accessed when the SPECEN flag is set. Write to HITCLR when SPECEN flag is set, resets all these registers.

REV $D015 (R)

Bit	7	6	5	4	3	2	1	0
	REV7	**REV6**	**REV5**	**REV4**	**REV3**	**REV2**	**REV1**	**REV0**

This register provides the revision ID of the SOPHIA's core. This register can only be accessed when the SPECEN flag is set.

PRIOR $D01B

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	Dir
SPECEN:0	**GTIAMOD1**	**GTIAMOD0**	**MCPLAY**	**FIFTHPL**	**PRIOR3**	**PRIOR2**	**PRIOR1**	**PRIOR0**	**W**
SPECEN:1	**VGA**	**RES2**	**RES1**	**RES0**	**PALE3**	**PALE2**	**PALE1**	**PALE0**	**R/W**
Initial	-	-	-	-	**0**	**0**	**0**	**0**	

Bit 7 – VGA

This flag sets the analog RGB video output to the VGA standard with H:31kHz; V:60/50Hz. The video mode is 480p/576p. This flag can only be accessed when the SPECEN flag is set.

Bits 6:4 – RES2:0 Resolution of the DVI video

These flags sets the DVI output resolution as follows:

RES2	RES1	RES0	Resolution	Aspect Ratio
0	0	0	480p/576p	3:2/5:4
0	0	1	1280x960	4:3
0	1	0	1280x1024	5:4
0	1	1	1344x960	14:10
1	0	0	1440x900	16:10
1	0	1	1536x960	16:10
1	1	0	1600x900	16:9
1	1	1	1704x960	16:9

These flags can only be accessed when the SPECEN flag is set.

Bits 3:0 – PALE3:0 Color Palette

These flags choose one of 16 active color palette. Palette #0 is default, standard PAL or NTSC palette. Palettes #1…15 are user programmable in the embedded RAM. These flags can only be accessed when the SPECEN flag is set. The composite and TV, PAL/NTSC encoded outputs uses always only default palette.

GRACTL $D01D

Bit	7	6	5	4	3	2	1	0	Dir
SPECEN:0	SPECEN	-	-	-	-	TRIGLEN	PLAYEN	MISSEN	W
SPECEN:1		SYNCTL	VGATE	HIRESBC	LUM0EN	INTERLACE	YUVRGB	NVEN	R/W
Initial	0	-	-	-	-	-	-	-	

Bit 7 – SPECEN: Special features enable

This flag, if set, enables an access to the SOPHIA special features flags. This flag, when clear, also resets the Palette RAM address counter.

Bit 6 – SYNCTL: SYNC Control

This flag controls the analog sync outputs as follows:

Mode	SYNCTL	H Output	V Output
RGB	0	CSYNC 0.3Vpp@75Ω	RGB Blanking
	1	HSYNC TTL	VSYNC TTL
VGA	X	HSYNC TTL	VSYNC TTL

This flag can only be accessed when the SPECEN flag is set.

Bit 5 – VGATE: Visible playfield gate

This flag, if set, limits the playfield width to 168 color cycles (336 high resolution pixels). This flag can only be accessed when the SPECEN flag is set.

Bit 4 – HIRESBC: Hi-Res Bi-Color

This flag, if set, enables bi-color high resolution graphics. The color of the graphics pixels is determined by the COLPF1 register, while the color of the playfield is determined by the COLPF2 register. This flag can only be accessed when the SPECEN flag is set.

Bit 3 – LUM0EN: LUM0 bit enable.

This flag, if set, enables 16 levels of luminance for all graphics modes. This flag can only be accessed when the SPECEN flag is set.

Bit 2 – INTERLACE

This flag controls the analog synchronization mode. When set, the interlaced mode is selected, otherwise the progressive mode. This flag can only be accessed when the SPECEN flag is set.

Bit 1 – YUVRGB

This flag controls the analog color space. When set, the RGB space is selected, otherwise the YPbPr space. This flag can only be accessed when the SPECEN flag is set.

Bit 0 – NVEN

This flag enables for a short time an access to the nonvolatile memory. Next write to the PMCTL or GTIACTL register will activate transfer of the current values of the red marked flags to the nonvolatile memory. Write operation must be executed within next 4 machine cycles after NVEN flag is set. This feature protects nonvolatile memory against a undesirable write operations. This flag can only be accessed when the SPECEN flag is set.

SOPHIA $D01E (R)

Bit	7	6	5	4	3	2	1	0
	SOPHIA7	**SOPHIA6**	**SOPHIA5**	**SOPHIA4**	**SOPHIA3**	**SOPHIA2**	**SOPHIA1**	**SOPHIA0**
Initial	0	1	0	1	0	0	1	1

This register indicates the SOPHIA 2 device presence. The constant value is 53 hex (“S”). This register can only be accessed when the SPECEN flag is set.

PALDATA $D01F (W)

This register is the Palette RAM data register. Each palette takes 768 bytes RAM. Each color is programmed in three consecutive bytes, as follows:

Bit	7	6	5	4	3	2	1	0
Lo	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	**x**	**x**
Med	**G5**	**G4**	**G3**	**G2**	**G1**	**G0**	**x**	**x**
Hi	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**x**	**x**

Each write cycle increments the address counter, therefore programming all 15 palettes requires 11520 write cycles. Address counter has a capacity of 12288 bytes. The last 768 bytes are unused. This register can only be accessed when the SPECEN flag is set. The SPECEN flag, when clear, also resets the address counter.